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10/750,001	12/30/2003	Sung-Kwon Lee	51876P507	9960

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EXAMINER	
JEFFERSON, QUOVAUNDA	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/750,001	Applicant(s) LEE ET AL.	
	Examiner Quovaunda Jefferson	**Art Unit** 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,31,32 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *various*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Response to Amendment

Applicant has amended claims 1, 3, 12, 14, 21, 23 and 31 and cancelled claims 30, 33-35, and 37-39. Claims 1-29, 31, 32, and 36 are pending in this application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-7, 10, 11, 31, 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) and Verret, US Patent

Application Publication 2001/0055840. See AAPA, Figures 1A-1D and Verret, Figure 12. For AAPA references, the application's publication, 2004/0253811.

FIG.1A
(PRIOR ART)

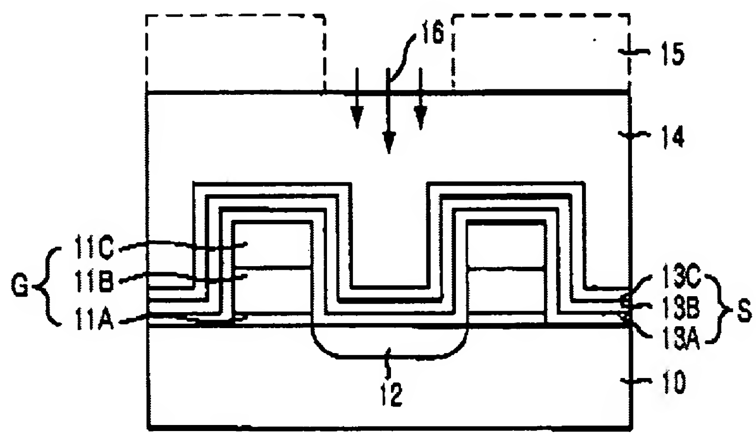


FIG.1B
(PRIOR ART)

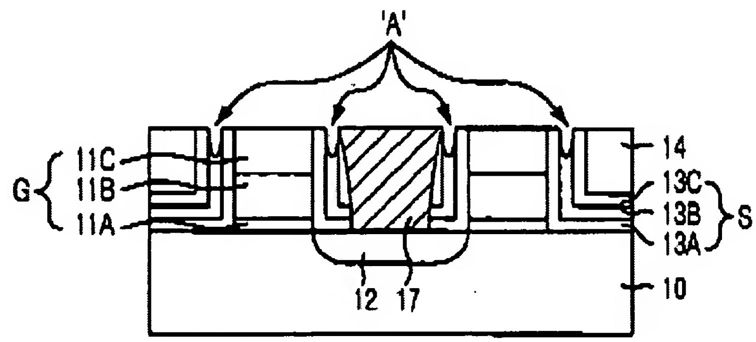


FIG.1C
(PRIOR ART)

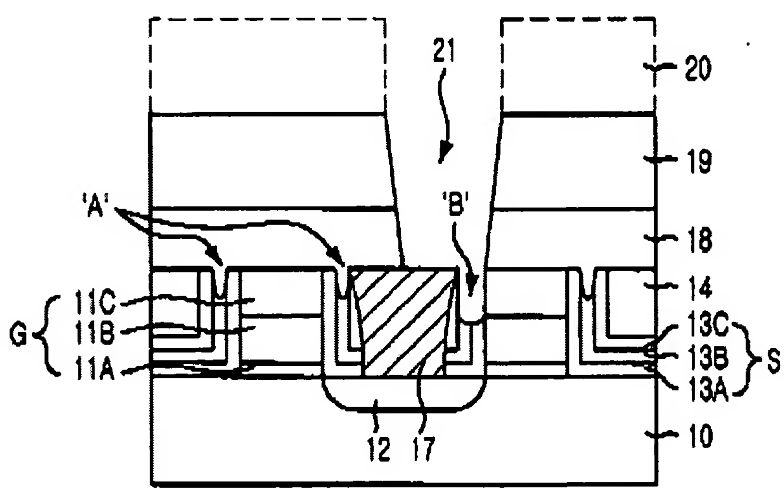


FIG.1D
(PRIOR ART)

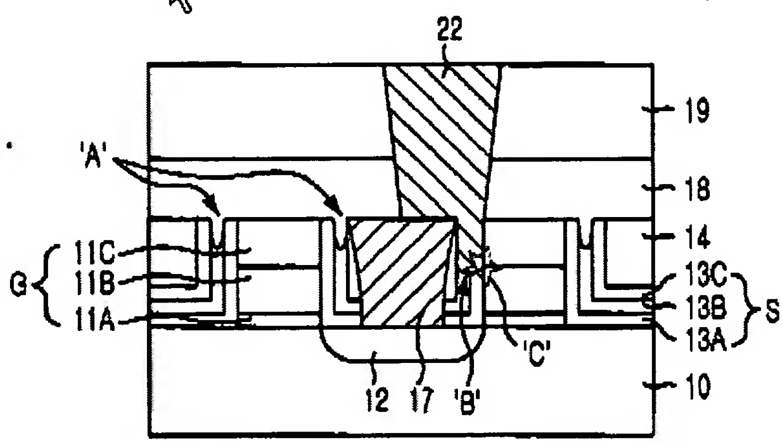
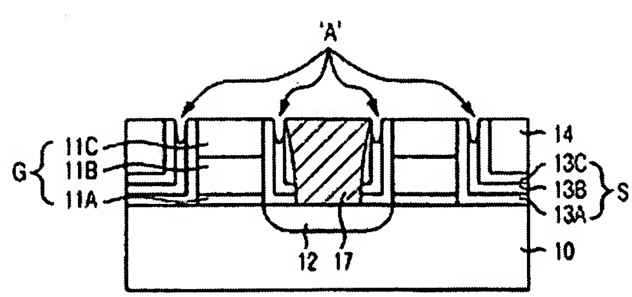


FIG.1B
(PRIOR ART)



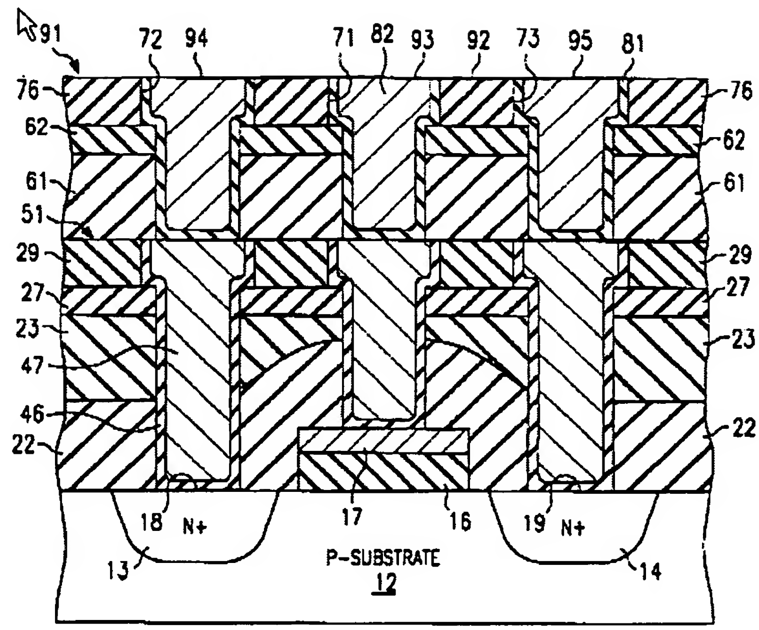


FIG. 12

Regarding claim 1, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate; etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1A), forming a first plug **17** by depositing a conductive layer on an entire surface of the resulting structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns (Figure 1B), etching selectively a second inter-layer insulation layer **18** deposited along a profile

containing the first plug to form a second contact hole exposing the first plug (Figure 1C); and forming a second plug electrically connected to the first plug through the second contact hole (Figure 1D).

AAPA fails to teach performing a cleaning process to remove remnants from the planarization process and an attack barrier layer is formed between the second plug and the conductive pattern. However, it is well known in the art to complete a post-planarization cleaning process. See US Patents 5,284,804; 5,607,341; and 5,780,364. Verret teaches an attack barrier layer **81** is formed between the second plug and the conductive pattern (while Verret does not show the attack barrier layer directly between the second plug and the conductive pattern, Verret teaches that an attack barrier layer can be disposed within a second plug. Therefore, the examiner takes the position that combining the teachings of the AAPA with that of Verret would result in an attack barrier layer formed between the second plug and the conductive pattern). It would be obvious to combine the teachings of Verret with that of the AAPA because the barrier layer promotes adhesion and serves as a diffusion barrier (Verret [0002]).

Regarding claim 3, AAPA further teaches the method as recited in claim 1, wherein the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior

to the step of performing the SAC etching process for forming the first contact hole (page 4).

Regarding claim 4, AAPA and Verret fail to teach the method as recited in claim 3, wherein in etching the partial portion of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern, the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern ranges from about 500 A to about 1500. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the

data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 5, Verrett teaches after the step of performing the cleaning process, the attack barrier layer **81** is deposited on an entire surface of the profile containing the first plug.

Regarding claim 6, Verret further teaches the method as recited in claim 1, wherein after the step of forming the second contact hole, the attack barrier layer is formed along a profile containing the second contact hole (Figure 12).

Regarding claim 7, Verret further teaches the method as recited in claim 1, wherein the attack barrier layer is a nitride-based layer [0023].

Regarding claim 10, AAPA further discloses the method as recited in claim 1, wherein the cleaning process uses a cleaning solution of hydrofluoric acid (HF) or buffered oxide etchant (BOE) [0014].

Regarding claim 11, AAPA further discloses the method as recited in claim 1, wherein the conductive pattern **G** is a gate electrode pattern and the second plug **22** is a storage node contact plug [0017].

Regarding claim 31, AAPA further discloses the method as recited in claim 1, wherein the second inter-layer insulation layer has a flow-fill property [0010].

Regarding claim 32, AAPA further discloses the method as recited in claim 31, wherein the second inter-layer insulation layer is made of an oxide-based material selected from a group consisting of advanced planarization layer (APL), spin on dielectric (SOD), spin on glass (SOG) and borophosphosilicate glass (BPSG) (Applicant admitted in prior art that the first inter-layer insulating layer can be made of an oxide based material, such as BPSG and APL. Therefore, the examiner takes the position that a second inter-layer insulation layer could me made of the same material as well) [0010].

Regarding claim 36, AAPA fails to disclose the method as recited in claim 31, wherein the second inter-layer insulation layer has a thickness ranging from about 1000 A to about 8000 A. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note

that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re* *Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Verret as applied to claim 1 above, and further in view of Vogel, "Modeled Tunnel Current for High Dielectric Constant Dielectrics", IEEE Transactions on Electrical Device.

Regarding claim 2, while AAPA discloses the method as recited in claim 1, wherein the multilayer structure of the etch stop layer includes nitride layers as top and

bottom most layers and at least one insulating material-based layer being disposed between the nitride layers, AAPA does not explicitly disclose at least one insulating material-based layer being disposed between the nitride layers having a lower dielectric constant than those of the nitride layers. Vogel teaches disclose at least one insulating material-based layer being disposed between the nitride layers having a lower dielectric constant than those of the nitride layers (see table II). It would be obvious to one skilled in the art to combine the teachings of Vogel with that of AAPA and Verret because the dielectric constant and barrier height can be used to calculate the tunneling current (Vogel).

Regarding claim 9, AAPA fails to disclose the method as recited in claim 2, wherein the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_20_3) layer and a tantalum oxynitride (TaON) layer. Vogel et al teaches insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_20_3) layer and a tantalum oxynitride (TaON) layer (Vogel, Table II).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Verret as applied to claim 1 above, and further in view of DeBoer et al, US Patent 6,696,336. AAPA and Verret fail to teach the method as recited in claim 1, wherein the attack barrier layer has a thickness ranging from about 50 A to about 500 A. DeBoer

teaches the attack barrier layer has a thickness ranging from about 50 A to about 500 A (column 4, line 60). It would have been obvious to one skilled in this art to combine the teachings of DeBoer with that of AAPA and Verret because the conductive digital plug [that is formed in this example] is protected by the dielectric layer (DeBoer, column 3, line 3-6).

Claims 12, 14-16, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) and Hiratani, US Patent Application Publication 2002/0074582. See Figures for AAPA and Hiratani. For AAPA references, the application's publication, 2004/0253811

Regarding claim 12, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate; etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1A); forming a first plug **17** by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns (Figure 1B), and etching selectively a second inter-layer insulation layer to form a second contact

hole exposing the first plug and forming a second plug electrically connected to the first plug through the second contact hole (Figure 1D).

AAPA fails to disclose performing a cleaning process to remove remnants from the planarization process and forming an attack barrier layer on an entire surface of the resulting structure including the first plug, a second inter-layer insulation layer formed on the attack barrier layer and etching selectively the attack barrier layer. However, it is well known in the art to complete a post-planarization cleaning process. See US Patents 5,284,804; 5,607,341; and 5,780,364. Hiratani teaches forming an attack barrier layer **37** on an entire surface of the resulting structure including the first plug **36**, a second inter-layer insulation layer **41** formed on the attack barrier layer and etching selectively the attack barrier layer. It would be obvious to one skilled in the art to combine the teachings of Hiratani with that of AAPA because the reliability of the semiconductor device can be improved (Hiratani, abstract).

Regarding claim 14, AAPA further discloses the method as recited in claim 12, wherein the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole.

Regarding claim 15, AAPA and Hiratani fail to teach the method as recited in claim 14, wherein in case of etching the partial portion of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern, the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern preferably ranges from about 500 A to about 1500 A.

However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka,* 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 16, Hiratani further teaches the method as recited in claim 12, wherein the attack barrier layer is a nitride-based layer [0101].

Regarding claim 19, AAPA discloses the method as recited in claim 12, wherein the cleaning process uses a cleaning solution of HF or BOE [0014].

Regarding claim 20, AAPA discloses the method as recited in claim 12, wherein the conductive pattern is a gate electrode pattern **G** and the second plug **22** is a storage node contact plug [0017].

Claims 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Hiratani as applied to claim 12 above, and further in view of Vogel et al, “Modeled Tunnel Current for High Dielectric Constant Dielectrics”, IEEE Transactions on Electrical Devices.

Regarding claim 13, while AAPA discloses the method as recited in claim 12, wherein the multi-layer structure of the etch stop layer includes nitride layers as top and

bottom most layers and at least one insulating material-based layer being disposed between the nitride layers, AAPA fails to discloses at least one insulating material-based layer being disposed between the nitride layers having a lower dielectric constant than those of the nitride layers. Vogel teaches disclose at least one insulating material-based layer being disposed between the nitride layers having a lower dielectric constant than those of the nitride layers (see table II). It would be obvious to one skilled in the art to combine the teachings of Vogel with that of Vogel with that of AAPA and Hiratani because the dielectric constant and barrier height can be used to calculate the tunneling current (Vogel).

Regarding claim 18, Vogel et al teaches insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an aluminum oxide (Al_20_3) layer and a tantalum oxynitride (TaON) layer (Table II).

Claims 21, 23-26, 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and DeBoer et al, US Patent 6,696,336. See AAPA and DeBoer Figures (DeBoer Figures are directly below).

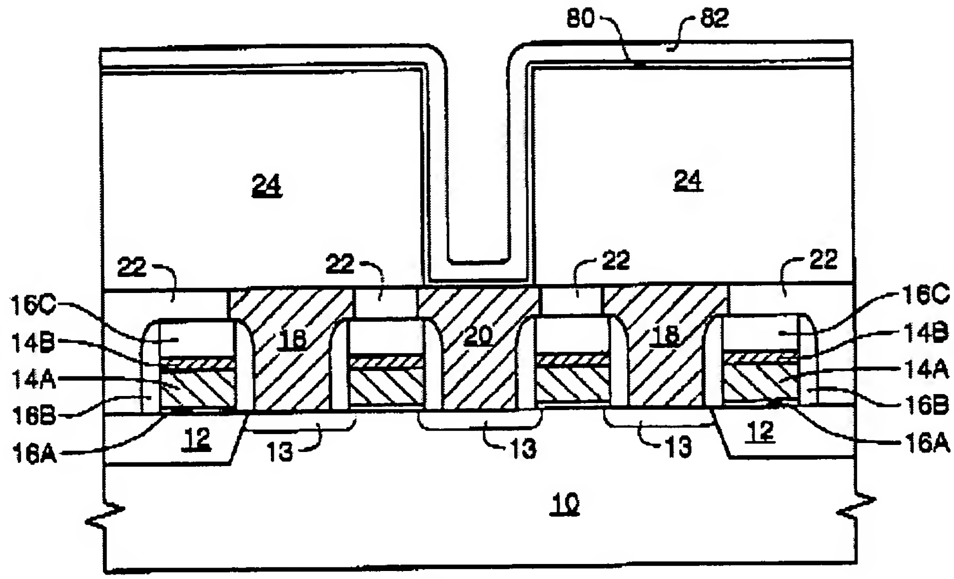


FIG. 8

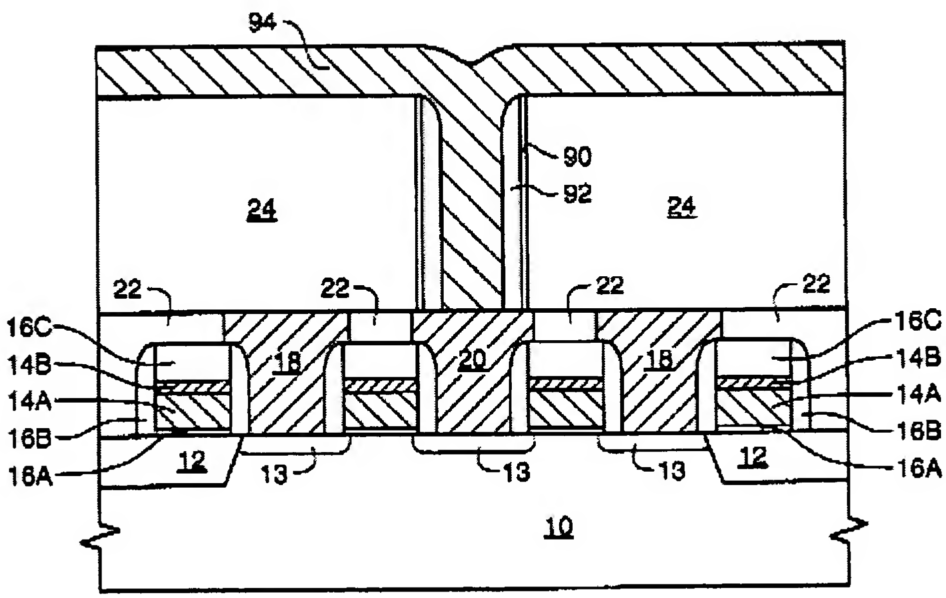


FIG. 9

DEBOER FIGURES

Regarding claim 21, AAPA discloses a method for fabricating a semiconductor device, comprising the steps of forming an etch stop layer **S** having a multi-layer structure along a profile containing conductive patterns **G** formed on a substrate (Figure 1A); etching selectively a first inter-layer insulation layer **14** deposited on the etch stop layer and the etch stop layer to form a first contact hole exposing a surface of the substrate allocated between the conductive patterns (Figure 1A); forming a first plug **17** by depositing a conductive layer on an entire surface of a structure containing the first contact hole and planarizing the conductive layer, the first inter-layer insulation layer and the etch stop layer at the same plane level of the conductive patterns and the first inter-layer insulation layer by employing a CMP process; and etching selectively a second inter-layer insulation layer deposited on the resulting structure including the first plug to form a second contact hole exposing the first plug (Figure 1C); and forming a second plug electrically connected to the first plug through the second contact hole (Figure 1D).

AAPA fails to disclose performing a cleaning process to remove remnants from the planarizing process and forming an attack barrier layer along a profile containing the second contact hole and removing the attack barrier layer disposed at a bottom surface of the second contact hole through an etch-back process. However, it is well known in the art to complete a post-planarization cleaning process. See US Patents 5,284,804; 5,607,341; and 5,780,364. DeBoer teaches forming an attack barrier layer **80, 82** along a profile containing the second contact hole and removing the attack barrier layer

disposed at a bottom surface of the second contact hole through an etch-back process (Figure 9). It would have been obvious to one skilled in the art to combine the teachings of the AAPA with that of DeBoer because the conductive digital plug (the second plug that is formed in this example) is protected by the dielectric layer (DeBoer, column 3, line 3-6).

Regarding claim 23, AAPA discloses the method as recited in claim 21, wherein the first inter-layer insulation layer and the etch stop layer disposed on an upper surface of each conductive pattern are etched by performing one of a plasma etching process with use of a mask opening only a cell region and a CMP process prior to the step of performing the SAC etching process for forming the first contact hole (page 4).

Regarding claim 24, AAPA and DeBoer fail to disclose the method as recited in claim 23, wherein in case of etching the partial portion of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern, the thickness of the first inter-layer insulation layer and the etch stop layer disposed on each conductive pattern preferably ranges from about 500 A to about 1500 A. However, given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved See *In re Aller, Lacey, and Hall* (10 USPQ 23 3-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of ether the critical nature of the claimed ranges or any unexpected results

arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that tile chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claim 25, DeBoer further teaches the method as recited in claim 21, wherein the attack barrier layer is a nitride-based layer (column 4, line 59).

Regarding claim 26, DeBoer further teaches the method as recited in claim 21, wherein the attack barrier layer has a thickness ranging from about 50 A to about 500 A (column 4, line 60).

Regarding claim 28, AAPA further teaches the method as recited in claim 21, wherein the cleaning process uses a cleaning solution of HF or BOE [0023].

Regarding claim 29, AAPA further teaches the method as recited in claim 21, wherein the conductive pattern **S** is a gate electrode pattern and the second plug **22** is a storage node contact plug [0017].

Claims 22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and DeBoer as applied to claim 12 above, and further in view of Vogel et al, "Modeled Tunnel Current for High Dielectric Constant Dielectrics", IEEE Transactions on Electrical Devices.

Regarding claim 22, AAPA and DeBoer fail to teach the method as recited in claim 21, wherein the multi-layer structure of the etch stop layer includes nitride layers as top and bottom most layers and at least one insulating material-based layer being disposed between the nitride layers and having a lower dielectric constant than those of the nitride layers. Vogel teaches disclose at least one insulating material-based layer being disposed between the nitride layers having a lower dielectric constant than those of the nitride layers (see table II). It would be obvious to one skilled in the art to combine the teachings of Vogel with that of Vogel with that of AAPA and DeBoer because the

dielectric constant and barrier height can be used to calculate the tunneling current (Vogel).

Regarding claim 27, Vogel teaches the insulating material-based layer having a lower dielectric constant than those of the nitride layers uses one of an oxide-based layer, an Al_2O_3 layer and a TaON layer (Table II).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quovaunda Jefferson whose telephone number is 571-272-5051. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qvj

W. DAVID COLEMAN
PRIMARY EXAMINER